IN THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as is shown below. The present listing of claims supersedes all previous versions and listings of claims in this application.

1. (Currently Amended) A digital signal processor ~~capable of performing~~ configured to perform a Viterbi algorithm, comprising:

an instruction fetching unit that fetches instructions;

a decoding unit that decodes the instructions fetched by the instruction fetching unit; and

an execution unit that executes the instructions decoded by the decoding unit, the execution unit comprising:

an arithmetic logic unit configured to perform a register-register arithmetic logic operation,

wherein the arithmetic logic unit compares a first data with a second data, in parallel with a comparison of a third data with a fourth data, and the execution unit outputs new path metrics; and

wherein each of the first data, the second data, the third data, and the fourth data ~~can each be~~ is one of four results obtained by adding one of two path metrics to one of two

branch metrics.

2. (Currently Amended) The digital signal processor according to claim 1, wherein the execution unit outputs any two new path metrics in a first part of data and in a second part of data, and wherein the first part of data is higher than the second part of data ~~high part and a low part of data outputted by the execution unit respectively~~.

3. (Original) The digital signal processor according to claim 2, wherein the execution unit compares the first data with the second data and compares the third data with the fourth data, and outputs new path metrics by one instruction.

4. (Currently Amended) A digital signal processor ~~capable of performing~~ configured to perform a Viterbi algorithm comprising:

an instruction fetching unit that fetches instructions;

a decoding unit that decodes the instructions fetched by the instruction fetching unit; and

an execution unit that executes the instructions decoded by the decoding unit, the execution unit comprising:

an arithmetic logic unit configured to perform a register-register arithmetic logic operation;

wherein the arithmetic logic unit compares a first data with a second data, in a single cycle that also includes a comparison of a third data with a fourth data, and the execution unit

outputs new path metrics, and

wherein each of the first data, the second data, the third data, and the fourth data ~~can each be~~ are one of four results obtained by adding one of two path metrics to one of two branch metrics.

5. (Original) The digital signal processor according to claim 4, wherein the execution unit outputs any two new path metrics in a high part and a low part of data outputted by the execution unit respectively.

6. (Original) The digital signal processor according to claim 5, wherein the execution unit compares the first data with the second data and compares the third data with the fourth data, and outputs new path metrics by one instruction.

7. (Currently Amended) The digital signal processor of claim 1,

wherein a ~~A~~ mobile station apparatus ~~comprising:~~ comprises the digital signal processor ~~of claim 1~~.

8. (Currently Amended) The digital signal processor of claim 1,

wherein a ~~A~~ base station apparatus ~~comprising:~~ comprises the digital signal processor ~~of claim 1~~.

9. (Cancelled)